VDU-G

Function.

This board provides storage for data to be displayed on a VDU and can also be accessed directly by a microprocessor.

Operation.

IC14 &16 are counters which continually generate the column and row numbers of the character to be displayed. The line counter IC14 is driven by the character clock (CCLK) and reset by the line delay (LSD). This counter also produces the end of line signal (EOL) when the count reaches 32. Similarly, IC16 counts the rows (RCLK) and produces an end of frame signal (EOF) at line 24 by using gates from IC15.

When the MPU wishes to access the video RAM, it sets the address bus to correspond to the video RAM address. When this condition is detected by IC17, the VS control line goes low and the multiplexers switch over so that the MPU address bus (AØ-9) is connected to the RAM address bus instead of the video address (AVØ-AV9) given by the counters. When the MPU has finished accessing the RAM, the VS line goes high again and normal character display continues under control of the counters. IC18 is used to complete decoding so that the video RAM is not selected when A8 &9 are both high. The multiplexers are also used to maintain the video RAM in a read only mode during VDU display, but allow the MPU to control the R/W line when appropriate.

IC12 & 13 provide bidirectional tri-state buffers from the video data to MPU data bus so that the two buses are isolated from one another until the MPU has control. Finally IC7 & 8 latch the video data from the RAM for output to the video character generator board (B).

Options.

VDU address.

The address of the VDU display RAM can be selected within a given page by linking the appropriate output from IC17 to VS, (marked Ø,4,8, C and VS on the layout). The board is prewired to locate the display at X4ØØ and this track should be cut when any other address is selected. If the whole system is using only a single 4K page of memory then the video RAM can be permanently enabled by wiring PS to GND. Otherwise the appropriate PS signal must be generated by external decoding.

JSD 10.12.78

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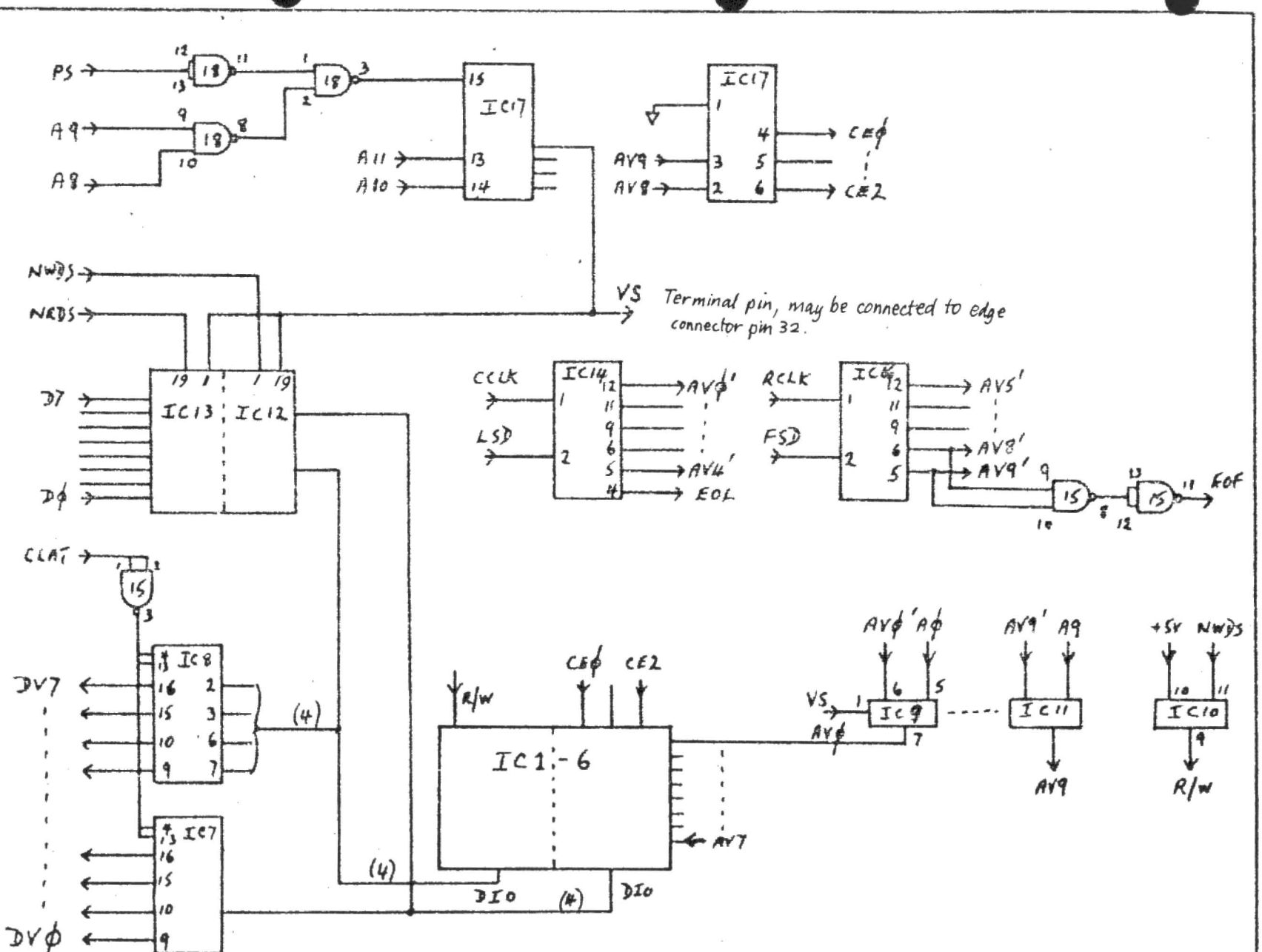
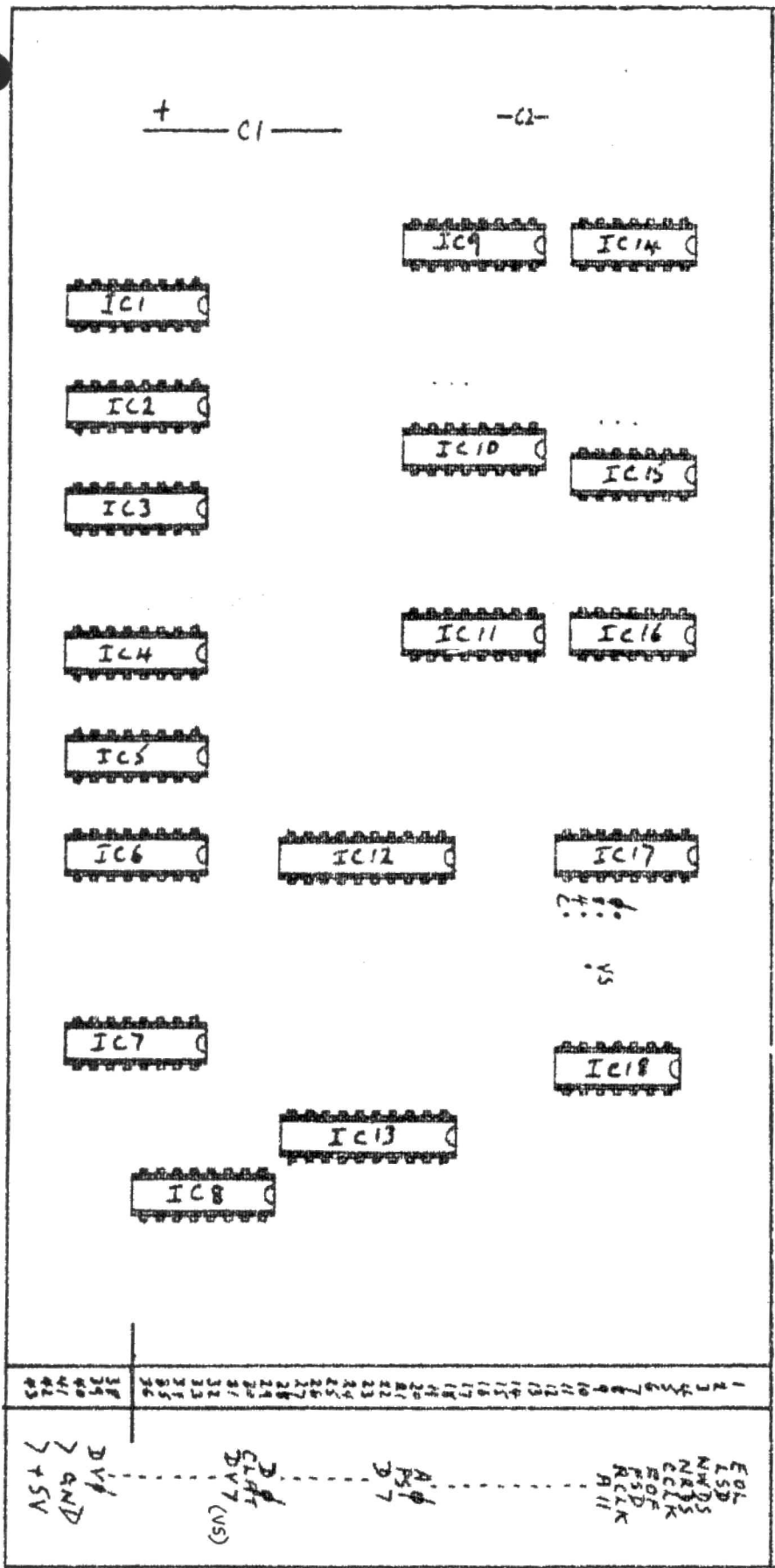
VDU-G-2

Drn. BSD

Date 6/12/79

REVN A 1979





COMPONENTS

C1	100μF 10V
2	0·1μ Disc

IC1-6	2112-2 (450nS)
7,8	7475
9-11	74LS157
12,13	81LS95
14,16	4024
15	74LS00
17	74LS139
18	74LS00

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